# Chapter 7

## The Serial Port Interface

128K
512K
512K E
+

## The SCC

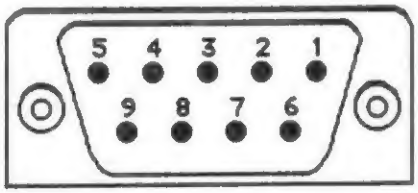
The two serial ports are controlled by a Zilog Z8530 **Serial Communications Controller** (SCC). The port known as SCC port A is the one with the modem icon on the back of the Classic Macintosh. SCC port B is the one with the printer icon.

Classic Macintosh serial ports conform to the EIA standard RS422, which differs from the more common RS232C standard. While RS232C modulates a signal with respect to a common ground ("single-ended" transmission), RS422 modulates two signals against each other ("differential" transmission). The RS232C receiver senses whether the received signal is sufficiently negative with respect to ground to be a logic "1", whereas the RS422 receiver simply senses which line is more negative than the other. This makes RS422 more immune to noise and interference, and more versatile over longer distances. If you ground the positive side of each RS422 receiver and leave unconnected the positive side of each transmitter, you've converted to EIA standard RS423, which can be used to communicate with most RS232C devices over distances up to fifty feet or so.

The serial inputs and outputs of the SCC are connected to the ports through differential line drivers (26LS30) and receivers (26LS32). The line drivers can be put in the high-impedance mode between transmissions, to allow other devices to transmit over those lines. A driver is activated by lowering the SCC's Request To Send (RTS) output for that port. Port A and port B are identical except that port A (the modem port) has a higher interrupt priority, making it more suitable for high-speed communication.

## SCC Connectors used on the Macintosh 128K, 512K , and 512K enchanced

The Macintosh 128K, 512K and the 512K enhanced use two DB-9 connectors for the two serial ports. Figure 7-1 shows the DB-9 pinout for the SCC serial connectors, and Table 7-1 gives the connections between the SCC Port (DB-9 connector) and the actual pin used on the SCC chip.




| | |
|---|---|
| 1 | Ground |
| 2 | +5 volts |
| 3 | Ground |
| 4 | Transmit data + |
| 5 | Transmit data - |
| 6 | +12 volts |
| 7 | Handshake/external clock |
| 8 | Receive data + |
| 9 | Receive data - |

**Figure 7-1**
Pinout for SCC DB-9 Output Jacks

**Table 7-1**
SCC Port (DB-9) Signal s connections to SCC Chip Pin Names

| Port Pin No. | Port Signal Abbreviation | Port Signal Name | SCC Chip Pin Name |
|---|---|---|---|
| 1 | Grnd | Ground | none |
| 2 | +5V | +5 Volts | none |
| 3 | Grnd | Ground | none |
| 4 | TXD+ | Transmit data + | $TxD_A$ |
| 5 | TXD— | Transmit Data — | $/RTS_A$ |
| 6 | +12V | +12 Volts | none |
| 7 | HSK/CLK | Handshake/External Clock | $CTS_A$ & $TRxC_A$ |
| 8 | RXD+ | Receive Data+ | $RxD_A$ |
| 9 | RXD— | Receive Data — | $RxD_A$ |

**Warning:**

Do not draw more than 100 milliamps at +12 volts, and 200 milliamps at +5 volts from all connectors combined.

Each port's input-only handshake line (pin 7) is connected to the SCC's Clear To Send (CTS) input for that port, and is designed to accept an external device's Data Terminal Ready (DTR) handshake signal. This line is also connected to the SCC's external synchronous clock (TRxC) input for that port, so that an external device can perform high-speed synchronous data exchange. Note that you can't use the line for receiving DTR if you're using it to receive a high-speed data clock.

The handshake line is sensed by the Classic Macintosh using the positive (noninverting) input of one of the standard RS422 receivers (26LS32 chip), with the negative input grounded. The positive input was chosen because this configuration is more immune to noise when no active device is connected to pin 7.

❖ *Note:* Because this is a differential receiver, any handshake or clock signal driving it must be "bi-polar", alternating between a positive voltage and a negative voltage, with respect to the internally grounded negative input. If a device tries to use ground (0 volts) as one of its handshake logic levels, the Classic Macintosh will receive that level as an indeterminate state, with unpredicatbale results.

The SCC itself (at its PCLK pin) is clocked at 3.672 megahertz (Clock signal name C3M). The internal synchronous clock (RTxC) pins for both ports are also connected to this 3.672 MHz clock. This is the clock that, after dividing by 16, is normally fed to the SCC's internal baud-rate generator.

The SCC chip generates level-1 processor interrupts during I/O over the serial lines. For more information about SCC interrupts, see *Inside Macintosh*.

The locations of the SCC control and data lines are given in the following table as offsets from the constant sccWBase for writes, or sccRBase for reads. These base addresses are also available in the global variables SCCWr and SCCRd. The SCC is on the upper byte of the data bus, so you must use only even-addressed byte reads (a byte read of an odd SCC read address tries to reset the entire SCC). When writing, however, you must use only *odd*-addressed byte writes (the MC68000 puts your data on both bytes of the bus, so it works correctly). A word access to any SCC address will shift the phase of the computer's high-frequency timing by 128 nanoseconds (system software adjusts it correctly during the system startup process).

| Location | Contents |
|---|---|
| sccWBase+aData | Write data register A |
| sccRBase+aData | Read data register A |
| sccWBase+bData | Write data register B |
| sccRBase+bData | Read data register B |
| sccWBase+aCtl | Write control register A |
| sccRBase+aCtl | Read control register A |
| sccWBase+bCtl | Write control register B |
| sccRBase+bCtl | Read control register B |

**Warning:**

Don't access the SCC chip more often than once every 2.2 usec. The SCC requires that much time to let its internal lines stabilize.

Refer to the technical specifications of the Zilog Z8530 for the detailed bit maps and control methods (baud rates, protocols, and so on) of the SCC.

Figure 7-2 shows a circuit diagram for the Classic Macintosh 128K, 512K and 512K enchanced serial ports.

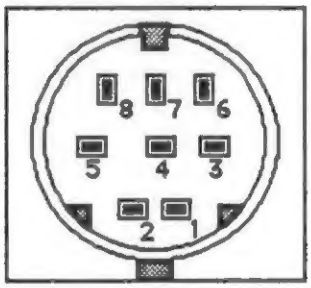
## SCC Connectors used on the Macintosh Plus

The Macintosh Plus uses two Mini-8 connectors for the two serial ports, replacing the two DB-9 connectors used for the serial ports on the Macintosh 128K, 512K, and 512K enhanced.

The Mini-8 connectors provide an output handshake signal, but do not provide the +5 volts and +12 volts found on the Macintosh 128K, 512K, and 512K enhanced serial ports.

The output handshake signal for each Macintosh Plus serial port originates at the SCC's Data Terminal Ready (DTR) output for that port, and is driven by an RS423 line driver.(Motorolla 3488A, or Fairchild 9636A) Other signals provided include input handshake/external clock, Transmit Data + and –, and Receive Data + and –.

Figure 7-3 shows the Mini-8 pinout for the SCC serial connectors, and Table 7-2 gives the connections between the SCC Port (DIN-8) and the actual pin used on the SCC chip.




1 Output handshake
2 Input handshake / external clock
3 Transmit data –
4 Ground
5 Receive data –
6 Transmit data +
7 (not connected)
8 Receive data +

Fig. 7-3

**Figure 7-3**
Pinout for SCC Serial Connectors

**Table 7-2**
SCC Port (Mini-8) Signal s connections to SCC Chip Pin Names

| Port Pin No. | Port Signal Abbreviation | Port Signal Name | SCC Chip Pin Name |
|---|---|---|---|
| 1 | $HSKo_A$ | Output Handshake | $/DTR_A$ |
| 2 | $HSKI_A$ | Input Handshake & External Clock | $CTS_A$ & $TRxC_A$ |
| 3 | $TXD_A-$ | Transmit data — | $TxD_A$ |
| 4 | Grnd | Ground | none |
| 5 | $RXD_A-$ | Receive Data - | $RxD_A$ |
| 6 | $TXD_A+$ | Transmit Data + | $/RTS_A$ |
| 7 | (not connected) | | |
| 8 | $RXD_A+$ | Receive Data+ | $RxD_A$ |

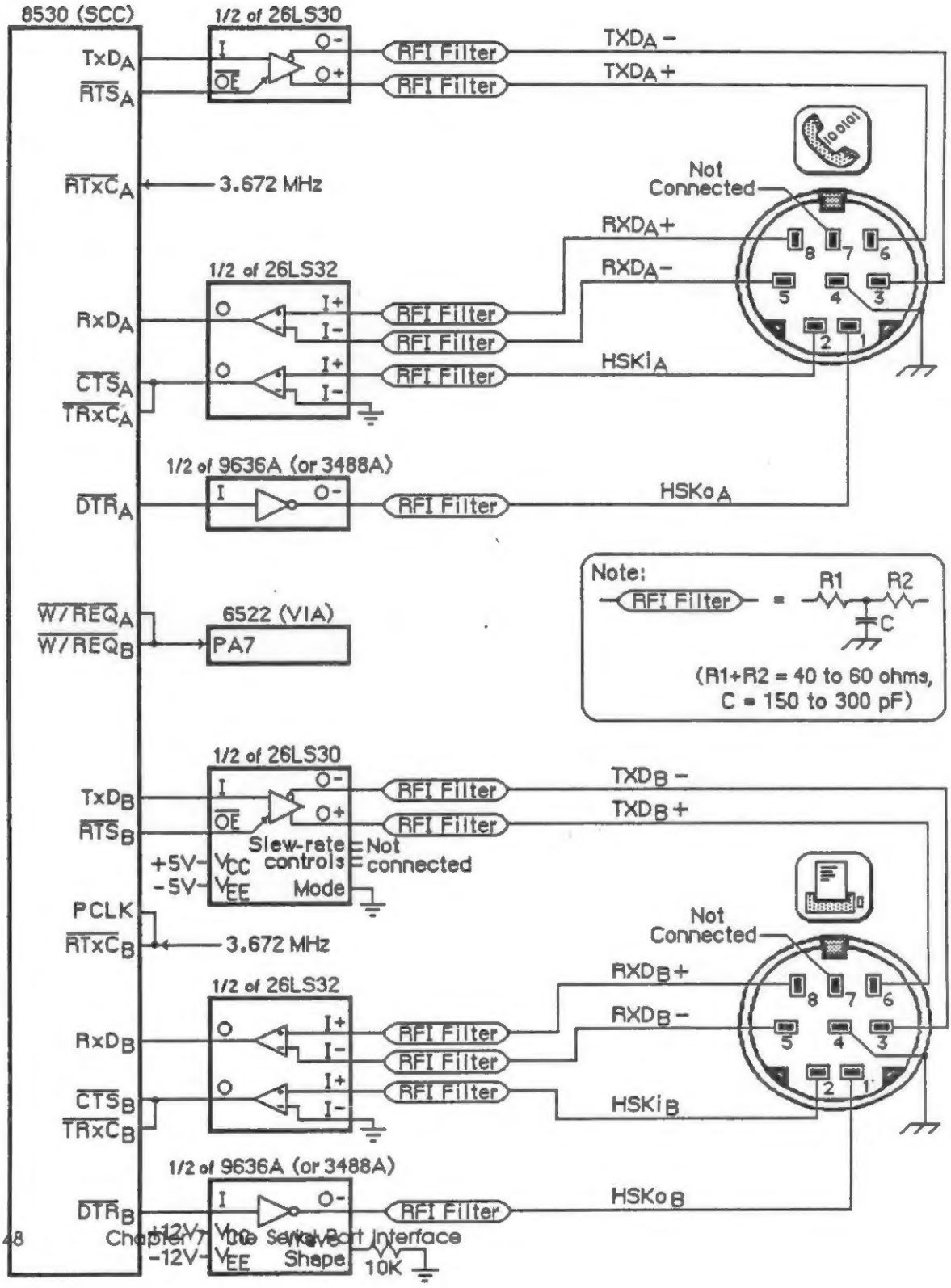

8530 (SCC)
1/2 of 26LS30
TxDA
RTSA
RFI Filter
TXDA –
TXDA +
RTxCA
3.672 MHz
Not Connected
RXDA+
RXDA–
1/2 of 26LS32
RxDA
CTSA
TRxCA
HSKiA
1/2 of 9636A (or 3488A)
DTRA
HSKoA
W/REQA
W/REQB
6522 (VIA)
PA7
Note:
R1
R2
C
(R1+R2 = 40 to 60 ohms,
C = 150 to 300 pF)
TxDB
RTSB
TXDB –
TXDB +
Slew-rate controls
Not connected
+5V
-5V
VCC
VEE
Mode
PCLK
RTxCB
3.672 MHz
RXDB+
RXDB–
RxDB
CTSB
TRxCB
HSKiB
DTRB
HSKoB
+12V
-12V
Drive Shape
10K

Fig. 7-4